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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,658	08/21/2003	Chunlin Liang	42P4516D2	9937

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EXAMINER

CHEN, ERIC BRICE

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/646,658

Applicant(s)

LIANG, CHUNLIN

Examiner

Eric B. Chen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 8/21/03.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 15-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 15-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>8/21/03</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Priority*

1. This application appears to be a division of Application No. 09/289,424, filed April 9, 1999. A later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in an earlier or parent application is known as a divisional application or "division." The divisional application should set forth the portion of the earlier disclosure that is germane to the invention as claimed in the divisional application.

### *Double Patenting*

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

3. A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

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4. Claim 26 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 12 of prior U.S. Patent No. 5,972,758, Liang. This is a double patenting rejection.

5. As to claim 26, Liang claims a method of forming an isolated junction comprising (column 6, line 25): a) lining vertical sidewalls of a trench formed in a surface of a semiconductor substrate with a spacer material (column 6, lines 27-28); b) isotropically etching the trench with an etchant that is more selective for the semiconductor substrate than for the spacer material, to form an undercut portion of the trench (column 6, lines 29-32); c) removing the remaining spacer material (column 6, line 33); d) oxidizing inner surface of the trench (column 6, line 34); e) forming air gaps in the undercut portion of the trench by partially filling trench with insulation material (column 6, lines 35-36); and f) implanting impurities into a portion of the semiconductor material that overlies the undercut portion of the trench (column 6, lines 37-39).

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

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7. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

8. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 15-25 are rejected under the judicially created doctrine of double patenting over claims 1-11 of U.S. Patent No. 5,972,758, Liang, since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

10. As to claim 15, Liang claims a method of forming an isolated junction field effect transistor comprising (column 5, lines 13-14): a) depositing a layer of trench masking material on a surface of a semiconductor substrate (column 5, lines 15-16); b) patterning the layer of trench masking material to expose portions of the semiconductor substrate (column 5, lines 17-18); c) etching the semiconductor substrate to form at least one trench, wherein each of the at least one trenches has a bottom surface and a side surface (column 5, lines 19-22); d) depositing a conformal layer of spacer material (column 5, line 24; Certificate of Correction); e) forming spacers adjacent to the trench side surfaces by anisotropically etching the spacer material until the semiconductor substrate at the bottom surface of the at least one trench is exposed (column 5, lines 25-28); f) isotropically etching the exposed semiconductor substrate (column 5, lines 29-30); g) filling each of the at least one trenches with at least one dielectric material

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(column 5, lines 32-33); h) forming a gate insulator layer (column 5, line 34); i) forming a gate electrode over the gate insulator layer (column 5, lines 35-36); and j) implanting impurities to form a source and a drain region (column 5, lines 37-38). Although the conflicting claims are not identical, they are not patentably distinct from each other because Applicant's claim 15 is generic to all that is recited in claim 1 of Liang. That is, claim 1 of Liang falls within the scope of Applicant's claim 15 or, in other words, Applicant's claim 15 is anticipated by claim 1 of Liang. Specifically, Liang claims "depositing a conformal layer of spacer material over at least the trench side surface" (column 5, line 24; Certificate of Correction). Applicant's claim 15 claims "depositing a conformal layer of spacer material," but does not does not require that the spacer material be formed "over at least the trench side surface."

11. As to claim 16, Liang claims that the depth of the trench is substantially equal to a predetermined junction depth (column 5, lines 39-40).

12. As to claim 17, Liang claims that the depth of the trench is greater than a predetermined junction depth (column 5, lines 41-42).

13. As to claim 18, Liang claims that the spacer layer material is a material selected from the group consisting of silicon oxide and silicon nitride (column 6, lines 1-3).

14. As to claim 19, Liang claims that filling each of the at least one trenches with at least one dielectric material comprises partially filling the undercut portions of the trenches with an oxide of silicon such that an air gap exists adjacent the stem portion of the T-shaped pedestal (column 6, lines 4-8).

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15. As to claim 20, Liang claims that prior to the step of filling each of the at least one trenches with at least one dielectric material, removing the spacers (column 6, lines 9-11).
16. As to claim 21, Liang claims that prior to the step of filling each of the at least one trenches with at least one dielectric material, thermally oxidizing inner surfaces of the at least one trench so as to form an oxide liner (column 6, lines 12-16).
17. As to claim 22, Liang claims that the gate insulator comprises an oxide of silicon (column 6, lines 17-18).
18. As to claim 23, Liang claims that the gate electrode comprises polysilicon (column 6, lines 19-20).
19. As to claim 24, Liang claims that the source and drain regions are doped with p type ions (column 6, lines 21-22).
20. As to claim 25, Liang claims that the source and drain regions are doped with n type ions (column 6, lines 23-24).

***Claim Rejections - 35 USC § 103***

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

22. Claims 15-18 and 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burton (U.S. Patent No. 4,888,300) in view of Streetman, *Solid State*

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*Electronic Devices*, Prentice Hall (1990) and Wolf et al., *Silicon Processing for the VLSI Era*, Vol. 1, Lattice Press (1986).

23. As to claim 15, Burton discloses a method of forming an isolated junction field effect transistor comprising: a) depositing a layer of trench masking material (16/18) (column 3, lines 20-25) on a surface of a semiconductor substrate (10/12) (column 3, lines 12-14) (Figure 1); b) patterning the layer of trench masking material to expose portions of the semiconductor substrate (column 3, lines 26-29); c) etching the semiconductor substrate to form at least one trench (20), wherein each of the at least one trenches has a bottom surface and a side surface (column 3, lines 29-32; Figure 2A); d) depositing a conformal layer of spacer material (24) (column 3, lines 47-52); e) forming spacers adjacent to the trench side surfaces by anisotropically etching the spacer material until the semiconductor substrate at the bottom surface of the at least one trench is exposed (column 3, lines 47-52); f) isotropically etching the exposed semiconductor substrate (column 4, lines 16-22); g) filling each of the at least one trenches with at least one dielectric material (column 4, lines 29-31); and h) forming a gate insulator layer (42) (column 4, lines 43-47).

24. Burton does not expressly disclose the step of: i) forming a gate electrode over the gate insulator layer. However, Burton teaches that standard bipolar, MOS or CMOS technology can further be applied to create a device on the isolated structure (column 4, lines 48-50). Streetman teaches that an established procedure for fabricating a MOS device includes forming a gate electrode ("poly-Si," Figure 8-26(a), page 324) over a gate oxide. Therefore, it would have been obvious to one of ordinary skill in the art at



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the time the invention was made to: form a gate electrode over the gate insulator layer.

One who is skilled in the art would be motivated to use an established procedure for forming a MOS device.

25. Burton does not expressly disclose the step of: j) implanting impurities to form a source and a drain region. However, Burton teaches that standard bipolar, MOS or CMOS technology can further be applied to create a device on the isolated structure (column 4, lines 48-50). Wolf teaches that ion implantation is used in source/drain formation in MOS devices (Table 1, page 281). Furthermore, Wolf teaches that ion implantation is primarily used to add dopant ions into the surface of silicon wafers and the technique is superior to chemical doping methods (page 280). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to: implant impurities to form a source and a drain region. One who is skilled in the art would be motivated to use a superior technique in forming source/drain regions in a MOS device.

26. As to claim 16, Burton discloses that the depth of the trench is substantially equal to a predetermined junction depth (column 3, lines 29-32).

27. As to claim 17, Burton does not expressly disclose that the depth of the trench is greater than a predetermined junction depth. At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to etch the depth of the trench is greater than a predetermined junction depth because applicant has not disclosed that etching the depth of the trench greater than a predetermined junction depth provides an advantage, is used for a particular purpose,

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or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with Burton's teachings because a trench depth substantially equal to a predetermined junction depth and a trench depth greater than a predetermined junction depth perform the same function.

28. As to claim 18, Burton discloses that the spacer layer material is a material selected from the group consisting of silicon oxide and silicon nitride (column 3, lines 47-48).

29. As to claim 20, Burton discloses that prior to the step of filling each of the at least one trenches with at least one dielectric material, removing the spacers (column 4, lines 16-26).

30. As to claim 21, Burton discloses that prior to the step of filling each of the at least one trenches with at least one dielectric material, thermally oxidizing inner surfaces of the at least one trench so as to form an oxide liner (34) (column 4, lines 28-29).

31. As to claim 22, Streetman discloses the gate insulator comprises an oxide of silicon (Figure 8-26(a), page 324).

32. As to claim 23, Streetman discloses the gate electrode comprises polysilicon (Figure 8-26(a), page 324).

33. As to claim 24, Streetman discloses the source and drain regions are doped with p type ions (Figure 8-26(a), page 324).

34. As to claim 25, Streetman does not expressly disclose that the source and drain regions are doped with p type ions. However, Streetman teaches that MOS transistors can either be of the n-type channel on a p-type Si substrate (page 300) or a p-type

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channel on a n-type substrate (page 301). Both n-channel and p-channel MOS transistors are commonly used. Moreover, forming a p-channel devices requires a p-type implant (page 301). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to: dope the source and drain regions with p type ions. One who is skilled in the art would be motivated to form a commonly used p-channel MOS transistor.

35. Claims 19 and 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burton in view of Wolf, in further view of Gardner et al. (U.S. Patent No. 6,268,637).

36. As to claim 19, Burton discloses filling each of the at least one trenches with at least one dielectric material comprises partially filling the undercut portions of the trenches with an oxide of silicon such that an air gap exists. Burton discloses forming an oxide of film (34) within cavity (32) (column 4, lines 28-29). Gardner discloses forming an isolation trench (26) to provide electrical isolation from circuit devices (18) and (20) (column 4, lines 3-6). Isolation trench (26) includes an air gap (26) (column 4, lines 34-51; Figure 3). Moreover, air gap (26) provides a structure with a dielectric constant of about 1.0 with reduced bulk (column 6, lines 33-38) as well as excellent electrical isolation (column 6, lines 43-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to: fill each of the at least one trenches with at least one dielectric material comprises partially filling the undercut portions of the trenches with an oxide of silicon such that an air gap exists. One who is skilled in the art would be motivated to form air gaps, due to the low dielectric constant and excellent electrical isolation characteristics.

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37. As to claim 26, Burton discloses a method of forming an isolated junction comprising: a) lining vertical sidewalls of a trench (20) formed in a surface of a semiconductor substrate with a spacer material (24) (column 3, lines 47-52); b) isotropically etching the trench with an etchant that is more selective for the semiconductor substrate than for the spacer material, to form an undercut portion of the trench (column 4, lines 16-26; Figure 8); c) removing the remaining spacer material (column 4, lines 16-26); and d) oxidizing inner surface of the trench (column 4, lines 28-29).

38. Burton does not expressly disclose: e) forming air gaps in the undercut portion of the trench by partially filling trench with insulation material. Burton discloses filling cavity (32) and trench (20) with polysilicon (column 4, lines 29-32). Gardner discloses forming an isolation trench (26) to provide electrical isolation from circuit devices (18) and (20) (column 4, lines 3-6). Isolation trench (26) includes an air gap (26) (column 4, lines 34-51; Figure 3). Moreover, air gap (26) provides a structure with a dielectric constant of about 1.0 with reduced bulk (column 6, lines 33-38) as well as excellent electrical isolation (column 6, lines 43-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to: form air gaps in the undercut portion of the trench by partially filling trench with insulation material. One who is skilled in the art would be motivated to form air gaps, due to the low dielectric constant and excellent electrical isolation characteristics.

39. Burton does not expressly disclose: f) implanting impurities into a portion of the semiconductor material that overlies the undercut portion of the trench. However,

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Burton teaches that standard bipolar, MOS or CMOS technology can further be applied to create a device on the isolated structure (column 4, lines 48-50). Wolf teaches that ion implantation is used in source/drain formation in MOS devices (Table 1, page 281). Furthermore, Wolf teaches that ion implantation is primarily used to add dopant ions into the surface of silicon wafers and the technique is superior to chemical doping methods (page 280). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to: implant impurities into a portion of the semiconductor material implanting impurities into a portion of the semiconductor material. One who is skilled in the art would be motivated to use a superior technique in forming source/drain regions in a MOS device.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC

April 12, 2005

*EBC*

NADINE G. NORTON  
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